REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

Disposition of Claims

Claims 1-13 were pending in the application. By way of this reply, claims 5, 7, and 12 have been cancelled without prejudice or disclaimer. Additionally, claims 14-17 have been newly added to the present application. Claims 1, 8, and 14 are independent. The remaining claims depend, directly or indirectly, from claims 1, 8, and 14.

Claim Amendments

Independent claims 1-4, 6, and 8-11 and 13 have been amended by way of this reply. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in paragraphs [0034]-[0037] of the present application.

Rejection(s) under 35 U.S.C § 112

Claims 1-6: 35 U.S.C. § 112, First Paragraph (First Rejection)

Claims 1-6 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Dependent claim 5 has been cancelled in this reply. Thus, this rejection is now moot with respect to claim 5. Claims 1-4 and 6 have been amended in this reply to clarify the present invention recited. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

The present invention is directed to a method and system for simulating an anti-resonance system of a section of a microprocessor. Amended independent claim 1 requires, in part, a simulated load that models a load of the anti-resonance circuit, a simulated transistor that models at least one high-frequency capacitance of the anti-resonance circuit, where the simulated transistor is connected in parallel with the simulated load, and a simulated capacitor that models an intrinsic capacitance of the section of the microprocessor, where the simulated capacitor is connected in parallel with the simulated load. Dependent claim 2 requires that the simulated load is a simulated resistor. Dependent claim 3 requires that the simulated resistor is a simulated voltage-controlled resistor. Dependent claim 4 requires that the anti-resonance circuit is simulated in synchronization with a simulated clock cycle. Dependent claim 6 requires that simulation of the anti-resonance circuit begins on a leading edge of the simulated clock cycle. Responses to the Examiner's questions will be considered in view of the above claim limitations and the Specification of the present invention.

3.1.1 Amended claim 1 is directed to a system for simulating an anti-resonance system of a section of a microprocessor. Accordingly, claim 1 requires a simulated load that is used to model a section of a microprocessor. A model is created, and the model is simulated. Results obtained from simulation are used to make design decisions for a microprocessor (*see* Specification, paragraph [0003]).

3.1.2 Amended claim 1 requires elements that are modeled to simulate various parts and characteristics of an anti-resonance circuit. For example, claim 1 requires, in part, a simulated load that models a load of the anti-resonance circuit. Thus, the apparatus describes a device comprising models of various elements for simulation. As discussed in the Specification and known by one skilled in the art, it is common to

use a model to simulate a system's performance to guide design decisions (*see* Specification, *e.g.*, paragraph [0003]).

3.1.3 As discussed with reference to Figure 5a of the present application, an actual anti-resonance circuit uses analog components to sense when the power supply collapses. However, it has been found that a power supply may begin to collapse at a leading edge of a clock cycle. Thus, simulation of a power supply anti-resonance circuit may begin on a simulated leading edge of a CPU clock cycle (*see* Specification, paragraph [0036]). One skilled in the art would appreciate that simulation of an electronic device, particularly a complex device such as a microprocessor, is a critical part in the design process of that device. Results of a simulation may include characteristics such as current or voltage at different locations. Characteristics such as these may be used to determine whether a given device or a part of a device is behaving properly in response to applied stimuli. One skilled in the art would appreciate that simulation of a device may be run in a number of ways and that outputs from such a simulation may be measured, recorded, and used to improve the design of the device in a number of ways. For example, input signals to a device may be simulated, and further, characteristics and responses of components of that device may also be simulated, resulting in one or more simulated output signals. Simulation of input signals, such as a clock signal, may occur in a number of ways. For example, a clock signal may be applied continuously throughout a simulation. One skilled in the art would appreciate that signals may be applied for a brief time, at regular or irregular intervals, or continuously throughout a simulation. Outputs of a simulation may be displayed in a readable form on a

computer screen, or in any number of other ways that allow design of the device to be improved.

3.1.4 An anti-resonance circuit is not used as a replacement for a decoupling capacitor. Figure 4 of the Specification shows a prior art approach of controlling parasitic inductance (*see* Specification, paragraph [0007]). Figure 5a shows a corresponding implementation of this approach (*see* Specification, paragraph [0009]). As discussed in paragraph [0017] of the present application, a circuit corresponding to this implementation charges and discharges as necessary to ensure stability in the power supply.

3.1.5 An anti-resonance circuit may provide stability for a power supply in a microprocessor. As discussed above, the present invention is directed to an apparatus and method for *simulating* an anti-resonance circuit of a section of a microprocessor, without reference to any other components in the microprocessor. Further, one skilled in the art would appreciate that while a specific number of components may be referenced in exemplary embodiments in the Specification, embodiments of the present invention may use any number of simulated anti-resonance circuits.

3.1.6 Specification, paragraph [0033] states:

While FIGS. 7a and 7b show nine bump and grid models 76a-76i, nine section models 80a-80i, and ten routing channels 82a-82l, it is fully intended that the scope of this invention covers embodiments with differing numbers of each of these components. For example, the chip could be represented by a four-by-four section model grid. The end result is that different arrangements and numbers of the component blocks shown in FIGS.

7a and 7b are dependent upon the components present in the system and are not limited to the embodiment shown here.

As discussed above, the present invention is not directed to an implementation of an anti-resonance system, but rather to a simulation. Accordingly, it would be obvious to one skilled in the art that specific numbers of models and components discussed in the Specification are used for exemplary purposes. Numbers discussed in the Specification could be altered as deemed appropriate by a designer of a microprocessor, and embodiments of the present invention are not limited to the numbers discussed in the exemplary embodiment of the present invention shown in Figures 7a and 7b of the Specification.

3.1.7 In one exemplary embodiment of the present invention, a section model, which represents a physical section of a chip, includes a load **86,** a transistor **88**, and a capacitor **90**. The load represents a load model for that section of the chip (*see* Specification, paragraphs [0034]-[0035]). As further discussed in paragraphs [0034]-[0035], an anti-resonance circuit may be simulated by a voltage-controlled resistor **92** for AC simulations. Thus, in one exemplary embodiment of the present invention, the load model represents a load of a simulated anti-resonance circuit of a microprocessor.

3.1.8 As discussed above, the present invention is directed to a simulation of an anti-resonance circuit of a microprocessor. One skilled in the art would appreciate that a simulated device may have multiple inputs and outputs. Thus, embodiments of the present invention may be coordinated with the simulation of other devices in a system. As further discussed above, one or more embodiments of the present invention may comprise nine section models and nine anti-resonance circuit models.

However, as clearly discussed in the Specification, embodiments of the present invention may have differing numbers of components. As embodiments of the present invention are used to simulate a real system, the component blocks exemplarily shown in Figures 7a and 7b are dependent on components present in a real system. Thus, the present invention is not limited to nine section models and nine anti-resonance circuits to simulate a microprocessor and an associated power system (*see, e.g.,* Specification, paragraph [0036]). One skilled in the art would appreciate that a number of variables may be applied to a simulated circuit, such as data signals, one or more clock signals, and power supply signals. However, decisions on how components are connected and simulated are made based on design considerations and results from simulations.

3.1.9 As discussed in the specification, transistor C_{LOCAL} **88** represents high-frequency capacitors local to an anti-resonance circuit. Such capacitance may be used to represent local high-frequency decoupling capacitors. As is well known to one skilled in the art, integrated circuits are often noisy. Capacitors may be used for a number of reasons in an integrated circuit, including for the reduction of noise internal to a circuit.

3.1.10 As discussed above, components used in a simulation may be chosen based on a number of design considerations. For example, as discussed above, in a section model in accordance with an embodiment of the present invention, a load model may use a simulated voltage-controlled resistor **92** to simulate an anti-resonance circuit of a microprocessor. Further, a simulated transistor C_{LOCAL} **88** may be used to simulate local high frequency decoupling capacitors, and a simulated voltage-controlled capacitor $C_{INTRINSIC}$ **90** may be used to simulate intrinsic

capacitances, such as intrinsic capacitance from transistors that would normally be present in a physical system.

3.1.11 Paragraph [0036] of the Specification states:

In an actual anti-resonance circuit, such as shown by example in FIG. 5a, the circuit itself uses analog components to sense when the power supply is collapsing. Once this collapse begins, the circuit then begins its charging/discharging to stabilize the supply. In the model, this analysis of the power supply is simulated by assuming when the collapse of the supply occurs. In general, it has been found that the supply begins to collapse at the beginning or leading edge of the CPU clock cycle.

As it has been found that a power supply collapse is likely to occur on a leading edge of a clock cycle, assuming that the collapse of the supply will occur on a leading edge allows greater simplification of the simulated circuit. Claim 4, as amended, requires that the anti-resonance circuit is simulated in synchronization with a simulated clock cycle. Claim 6, as amended, requires that simulation of the anti-resonance circuit begins on a leading edge of the simulated clock cycle. In other words, a simulated clock cycle is used in the simulation of the anti-resonance circuit. Further, simulation of the anti-resonance circuit begins on a leading edge of a clock cycle. Figure 10 shows a graph of a CPU clock cycle **94** in accordance with one embodiment of the present invention. As discussed with reference to paragraph [0036] of the present application, the leading edge **96** of the first cycle is a point where simulation of collapse of the supply, and resultantly the anti-resonance circuit, could begin.

Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, first paragraph, claims 1-4 and 6 do not contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Accordingly, withdrawal of the § 112 rejections of claims 1-4 and 6 is respectfully requested.

Claim 7: 35 U.S.C. § 112, First Paragraph (First Rejection)

Claim 7 was rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 7 has been cancelled in this reply. Thus, this rejection is now moot with respect to claim 7. Accordingly, withdrawal of the rejection is respectfully requested.

Claims 8-13: 35 U.S.C. § 112, First Paragraph (First Rejection)

Claims 8-13 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 12 has been cancelled in this reply. Thus, this rejection is now moot with respect to claim 12. Claims 8-11 and 13 have been amended in this reply to clarify the present invention recited. The Examiner asserts that claims 8-13 are method claims having the same limitations as the apparatus claims 1-6, and raise the same issues as claims 1-6. As claims 1-4 and 6 have been shown to be patentable above, claims 8-11 and 13 are patentable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 1-6: 35 U.S.C. § 112, First Paragraph (Second Rejection)

Claims 1-6 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art to which it pertains, or with which it was most nearly connected, to make and/or use the invention. Dependent claim 5 has been cancelled in this reply. Thus, this rejection is now moot with respect to claim 5. Claims 1-4 and 6 have been amended in this reply to clarify the present invention recited. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

The Examiner has raised the same issues with reference to this § 112 rejection as in the previous § 112 rejection. As claims 1-4 and 6 were shown to be patentable above, withdrawal of this rejection is respectfully requested.

Claim 7: 35 U.S.C. § 112, First Paragraph (Second Rejection)

Claim 7 was rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art to which it pertains, or with which it was most nearly connected, to make and/or use the invention. Claim 7 has been cancelled in this reply. Thus, this rejection is now moot with respect to claim 7. Accordingly, withdrawal of the rejection is respectfully requested.

Claims 8-13: 35 U.S.C. § 112, First Paragraph (Second Rejection)

Claims 8-13 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art to which it pertains, or with which it was most nearly connected, to make and/or use the invention. Claim 12 has been cancelled in this reply. Thus, this rejection is now moot with respect to claim 12. Claims 8-11 and 13 have been amended in this reply to

clarify the present invention recited. The Examiner asserts that claims 8-13 are method claims having the same limitations as the apparatus claims 1-6, and raise the same issues as claims 1-6. However, the Examiner has raised the same issues with reference to this § 112 rejection as in the previous § 112 rejection. As claims 1-4 and 6 were shown to be patentable above, claims 8-11 and 13 are patentable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 1-6: 35 U.S.C. § 112, Second Paragraph (First Rejection)

Claims 1-6 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Dependent claim 5 has been cancelled in this reply. Thus, this rejection is now moot with respect to claim 5. Claims 1-4 and 6 have been amended in this reply to clarify the present invention recited. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

As discussed above, amended independent claim 1 is directed to an apparatus for simulating an anti-resonance circuit of a section of a microprocessor that comprises, in part, a simulated load that models a load of the anti-resonance circuit, a simulated transistor that models at least one high-frequency capacitance of the anti-resonance circuit, where the simulated transistor is connected in parallel with the simulated load, and a simulated capacitor that models an intrinsic capacitance of the section of the microprocessor, where the simulated capacitor is connected in parallel with the simulated load.

From amended claim 1, it is now clear the present invention is directed to a simulation tool that comprises a number of simulated components, for example, a simulated load, a simulated transistor, and a simulated capacitor. Paragraph [0035] clearly states that the anti-

resonance circuit is simulated by voltage-controlled resistor in the exemplary embodiment shown in Figure 9 of the Specification.

Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claims 1-4 and 6 are not indefinite. Accordingly, withdrawal of the § 112, second paragraph, rejections of claims 1-4 and 6 is respectfully requested.

Claim 7: 35 U.S.C. § 112, Second Paragraph (First Rejection)

Claim 7 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 has been cancelled in this reply. Thus, this rejection is now moot with respect to claim 7. Accordingly, withdrawal of the rejection is respectfully requested.

Claims 8-13: 35 U.S.C. § 112, Second Paragraph (First Rejection)

Claims 8-13 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 12 has been cancelled in this reply. Thus, this rejection is now moot with respect to claim 12. Claims 8-11 and 13 have been amended in this reply to clarify the present invention recited. The Examiner asserts that claims 8-13 are method claims having the same limitations as the apparatus claims 1-6, and raise the same issues as claims 1-6. As claims 1-6 have been shown to be patentable above, claims 8-11 and 13 are patentable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Claim 1: 35 U.S.C. § 112, Second Paragraph (Second Rejection)

Claim 1 was rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential structural cooperative elements, such omission amounting to a gap between

the necessary structural connections. Claim 1 has been amended in this reply to clarify the present invention recited. To the extent that this rejection may still apply to the amended claim, the rejection is respectfully traversed.

Amended claim 1 is directed to an apparatus for simulating an anti-resonance circuit of a section of a microprocessor and requires, in part, a processor and memory. As discussed above with reference to the section titled "Claims 1-6: 35 U.S.C. § 112, First Paragraph (First Rejection," it would be clear to one skilled in the art that recording and displaying outputs of the simulation, as well as other means for performing other functions may be necessary. Thus, with respect to the Examiner's rejection under 35 U.S.C. § 112, second paragraph, claim 1 is not incomplete. Accordingly, withdrawal of the § 112, second paragraph, rejection of claim 1 is respectfully requested.

Claim 7: 35 U.S.C. § 112, Second Paragraph (Second Rejection)

Claim 7 was rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential structural cooperative elements, such omission amounting to a gap between the necessary structural connections. Claim 7 has been cancelled in this reply. Thus, this rejection is now moot with respect to claim 7. Accordingly, withdrawal of the rejection is respectfully requested.

Claim 8: 35 U.S.C. § 112, Second Paragraph (Second Rejection)

Claim 8 was rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. Claim 8 has been amended in this reply to clarify the present invention recited. To the extent that this rejection may still apply to the amended claim, the rejection is respectfully traversed.

Amended claim 8 is directed to a method for simulating an anti-resonance circuit of a section of a microprocessor, comprising simulating a load of the anti-resonance circuit, simulating at least one high frequency capacitance of the anti-resonance circuit in parallel with the simulated load, and simulating a section of the microprocessor's intrinsic capacitance in parallel with the simulated load.

As discussed above, it would be obvious to one skilled in the art that a number of steps are required to perform a simulation. However, the present invention is directed to a method and apparatus for simulating an anti-resonance circuit of a section of a microprocessor. Accordingly, the necessary steps have been recited in amended claim 8. Thus, with respect to the Examiner's rejection under 35 U.S.C. § 112, second paragraph, claim 8 is not incomplete. Accordingly, withdrawal of the § 112, second paragraph, rejection of claim 8 is respectfully requested.

Rejection(s) under 35 U.S.C § 101

Claims 1-7 were rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Independent claim 1 has been amended in this reply in view of this rejection. Claims 5 and 7 have been cancelled in this reply. Thus, this rejection is now moot with respect to claims 5 and 7. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

As amended, claim 1 requires, in part, a processor and memory to perform the necessary functions related to simulating an anti-resonance circuit of a section of a microprocessor. The processor and memory are hardware components which will implement necessary software components. Thus, claim 1 is not directed to non-statutory subject matter,

and claim 1 is patentable. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of the § 101 rejections of claims 1-4 and 6 is respectfully requested.

Rejection(s) under 35 U.S.C § 103

As an initial matter, Applicant notes that various combinations of one or more of ***eight*** references have been used in rejecting the claims of the present application. The purported reconstruction of the claimed invention by reliance on such a large number of references ranging among various technologies is not appropriate. It is abundantly clearly that the Examiner, using the present application as a guide, has selected isolated features of the various relied-upon references to arrive at the limitations of the claimed invention. Use of the present application as a "road map" for selecting and combining prior art disclosures is wholly improper. *See Interconnect Planning Corp. v. Feil*, 774 F.2d 1132 (Fed. Cir. 1985) (stating that "[t]he invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time"); *In re Fritch*, 972 F.2d 1260 (Fed. Cir. 1992) (stating that "it is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious . . . . This court has previously stated that 'one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.'"); *In re Wesslau*, 353 F.2d 238 (C.C.P.A. 1965) (stating that "it is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art").

Claims 1, 2, 8, and 9

Claims 1, 2, 8, and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Larsson ("Resonance and Damping in CMOS Circuits with On-Chip Decoupling

Capacitance," Patrik Larsson, IEEE Transactions on Circuits and Systems, August 1998, pages 849-858) in view of U.S. Patent No. 6,240,246 issued to Evans (hereinafter "Evans") and U.S. Patent No. 3,808,370 issued to Jackson et al. (hereinafter "Jackson"), and further in view of U.S. Patent Application Publication No. 2002/0011885 in the name of Ogawa et al. (hereinafter "Ogawa") and Herrell et al. ("Modeling of Power Distribution Systems for High-Performance Microprocessors," Dennis J. Herrell and Benjamin Baker, IEEE Transactions on Advanced Packaging, August 1999, pages 240-248). Claims 1, 2, 8, and 9 have been amended by this reply. To the extent that this rejection may apply to the amended claims, the rejection is respectfully traversed.

The present invention is directed to an apparatus and a technique for simulating an anti-resonance circuit of a section of a microprocessor. The technique uses a simulated load that models a load of the anti-resonance circuit, a simulated transistor that models at least one high-frequency capacitance of the anti-resonance circuit, and a simulated capacitor that models an intrinsic capacitance of the section of the microprocessor. The simulated transistor and the simulated capacitor are connected in parallel with the simulated load.

As discussed with reference to an exemplary embodiment of the present invention shown in Figure 8 of the Specification, the simulated model, representing a physical section of a chip, includes a simulated load **86** (representing a load model for that section of the chip) that is connected in parallel to a simulated transistor C_{LOCAL} **88** and a simulated voltage-controlled capacitor $C_{INTRINSIC}$ **90** (*see* Specification, e.g., paragraph **[0034]**). The simulated load may be a voltage controlled resistor, which represents the anti-resonance circuit (*see* Specification, e.g., paragraph **[0035]**). C_{LOCAL} **88** and $C_{INTRINSIC}$ **90** simulate local high-frequency capacitors and the intrinsic transistor capacitance of the section of the chip, respectively. The values of the simulated load **86**, the simulated transistor C_{LOCAL} **88**, and the simulated capacitor $C_{INTRINSIC}$ **90**

are selected to accurately simulate the performance of specific modeled components (*see* Specification, e.g., paragraph [**0034**]).

The simulation of an anti-resonance circuit of a section of a microprocessor in accordance with the present invention provides low complexity with a simulation time that may be orders of magnitude faster than a model that uses transistors. Further, the model provides flexibility in accurately modeling system performance in AC analysis (*see* Specification, e.g., paragraph [**0037**]).

Larsson discloses the use of a model to predict the resonance frequency of a CMOS circuit (*see* Larsson, *e.g.,* page 849, col. 2, paragraph 1, lines 1-7). Through the use of a model, Larsson simplifies a complex CMOS circuit into RC networks and further to a simple second-order system in order to estimate the resonance frequency of the circuit (*see* Larsson, *e.g.,* page 857, col. 1, paragraph 2, lines 1-4). Larsson also proposes design techniques to control resonance and increase damping in a CMOS circuit (*see* Larsson, *e.g.,* page 849, col. 1, paragraph 3, lines 11-13). However, Larsson is silent with respect to discussion of simulating an anti-resonance circuit of a section of a microprocessor, as required by independent claims 1 and 8 of the present application. Larsson does not disclose, or otherwise teach, at least the limitations of independent claims 1 or 8 of the present application

Evans discloses a device for filtering feedback signals available in an electromechanical actuation system (*see* Evans, *e.g.,* col. 1, lines 16-19). In Evans, a method for filtering oscillations in a closed loop control system for controlling the movement of a structure is disclosed. Evans is completely silent with respect to simulating a circuit, and specifically with respect to an apparatus or method for simulating an anti-resonance circuit of a section of a microprocessor. Like Larsson, Evans does not disclose, or otherwise teach, at least the limitations of independent claims 1 or 8 of the present application.

As discussed above, Larsson uses a model to predict the resonance frequency of a CMOS circuit. Larsson is silent with respect to simulating an anti-resonance circuit of a microprocessor. Jackson is directed to a system using adaptive filters for detecting formant information in speech and in determining pitch and/or anti-resonance information (*see* Jackson, *e.g.,* col. 1, lines 47-51). As shown below, Jackson cannot be combined with Larsson.

Jackson references U.S. Patent No. 3,190,963 ("the '363 Patent"), which clearly states that in voice applications, anti-resonant frequencies correspond to regions of relatively ineffective transmission through a talker's vocal tract (*see* the '363 Patent, *e.g.,* col. 1 lines 48-50). Thus, the anti-resonant information of Jackson has no connection to the present invention. Jackson states that an object of the invention disclosed therein is to determine pitch or anti-resonance information, but this relates to voiced speech. Jackson provides no motivation for simulating an anti-resonance circuit of a microprocessor. Like Larsson and Evans, Jackson does not disclose, or otherwise teach, at least the limitations of independent claims 1 and 8 of the present application.

Ogawa discusses a transistor description format that allows the internal circuit configurations of a large scale integrated circuit to be accurately described with transistor models, interconnection resistance models, and capacitance models (*see* Ogawa, *e.g.,* page 1, Para 0007, lines 7-11). Ogawa does not discuss simulating a high-frequency capacitance with a simulated transistor. Further, like Larsson, Evans, and Jackson, Ogawa does not disclose, or otherwise teach, at least the limitations of independent claims 1 and 8 of the present application.

In view of the above, Larsson, Evans, Jackson, Ogawa, and Herrell, whether considered separately or in any combination, fail to disclose all the limitations of independent claims 1 and 8 of the present application. Additionally, there is no motivation to combine the references contained within the references themselves.

In view of the above, Larsson, Evans, Jackson, Ogawa, and Herrell, whether taken separately or in combination, (i) are not combinable, and (ii) fail to show or suggest the present invention as recited in amended independent claims 1 and 8. Thus, amended independent claims 1 and 8 are patentable over Larsson, Evans, Jackson, Ogawa, and Herrell. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 3 and 10

Claims 3 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Larsson in view of Evans and Jackson, and further in view of Ogawa, Herrell, and U.S. Patent No. 4,459,566 issued to Lane (hereinafter "Lane"). Claims 3 and 10 have been amended by this reply. To the extent that this rejection may apply to the amended claims, the rejection is respectfully traversed.

As discussed above, Larsson, Evans, Jackson, Ogawa, and Herrell fail to show or suggest all the limitations of claims 1 and 8 of the present invention. Lane fails to disclose all the limitations of claims 1 or 8 or supply that which the above references lack. It is asserted that Lane teaches that the resistor is a voltage controlled resistor (page 9, section 8.1). This is not correct. The device of Lane is a voltage controlled **oscillator** (VCO) (*see* Lane, *e.g.*, col. 1, lines 51-62). Lane is directed to a VCO having a particular center frequency about which the output frequency is varied in response to an input control signal (*see* Lane, col. 1, lines 13-17). A VCO, as explained by Lane, provides an output signal having a **frequency** proportional to the magnitude of an input control signal. The oscillator employs a circuit that simulates a resistance-inductance-capacitance (RLC) circuit that is adjustable in response to the input control signal. Further, the above cited references provide no motivation, and the Applicant knows of none, as

to why one skilled in the art would seek the teachings of Lane in light of the above cited references in regard to a VCO, which is not relevant to the present invention.

Therefore, like Larsson, Evans, Jackson, Ogawa, and Herrell, Lane does not disclose, or otherwise teach, at least the limitations of independent claims 1 and 8 of the present application. Accordingly, because independent claims 1 and 8 have been shown to be patentable, claims 3 and 10 are patentable for at least the same reasons.

Claims 4, 5, 11, and 12

Claims 4, 5, 11, and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Larsson in view of Evans and Jackson, and further in view of Ogawa, Herrell, and U.S. Patent No. 6,370,678 issued to Culler (hereinafter "Culler"). Claims 5 and 12 have been cancelled by this reply. Accordingly, the rejections with respect to claims 5 and 12 are now moot. Claims 4 and 11 have been amended by this reply. To the extent that this rejection may still apply to the amended claims, this rejection is respectfully traversed.

Like Larsson, Evans, Jackson, Ogawa, and Herrell, Culler fails to disclose all the limitations of independent claims 1 and 8 of the present application or supply that which the others lack. The device of Culler uses circuit simulations on models of power supply circuits to determine the primary resonant frequencies identified with each of the power supply circuits. These resonant frequencies are used as input to the initial floor planning (*see* Culler, col. 4, lines 53-59). Culler discloses that these models and the identification of resonant frequencies can be used to develop design constraints supplied as input to the logic synthesis process (*see* Culler, abstract). There is no disclosure in Culler of anti-resonance circuit designs for microprocessors. Accordingly, Culler cannot simulate an anti-resonance circuit of a section of a microprocessor.

Therefore, like Larsson, Evans, Jackson, Ogawa, and Herrell, Culler does not disclose, or otherwise teach, at least the limitations of independent claims 1 and 8 of the present

application. Accordingly, because independent claims 1 and 8 have been shown to be patentable, claims 4 and 11 are patentable for at least the same reasons.

Claims 6 and 13

Claims 6 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Larsson in view of Evans and Jackson, and further in view of Ogawa, Herrell, Culler, and U.S. Patent 5,223,653, issued to Kunimoto et al. (hereinafter "Kunimoto"). Claims 6 and 13 have been amended by way of this reply. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

Kunimoto is directed to a musical tone synthesizing apparatus. In Figure 1 of Kunimoto, Kunimoto refers to a resonance circuit comprising an adder **1**, a delay circuit **2**, and a filter **3**. As explained by Kunimoto, characteristics of these circuit elements are determined in response to a desired musical instrument to be simulated (*see* Kunimoto, col. 1, lines 29-37). Applicant knows of no reason as to why one skilled in the art would seek the teachings of Kunimoto, which is not relevant to the present invention, in light of the above cited references. Kunimoto is **completely** silent with respect to simulating an anti-resonance circuit of a section of a microprocessor.

Like Larsson, Evans, Jackson, Ogawa, Herrell, and Culler, Kunimoto does not disclose, or otherwise teach, at least the limitations of independent claims 1 and 8 of the present application. Accordingly, because independent claims 1 and 8 have been shown to be patentable, claims 6 and 13 are patentable for at least the same reasons.

Claim 7

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Larsson in view of Evans and Jackson, and further in view of Culler. Claim 7 has been cancelled by way

of this reply. Thus, the rejection is now moot with respect to claim 7. Accordingly, withdrawal of this rejection is respectfully requested.

Response to Arguments

In section 27 of the Office Action of January 14, 2005 ("Office Action"), the Examiner repeats a number of questions that were addressed in section 3 of the Office Action. Accordingly, responses to these questions are incorporated from the corresponding section of this response. Further, Applicant respectfully notes that the Examiner has failed to address arguments in the previous response concerning the lack of combinability of the prior art references and the lack of motivation to combine the prior art references. Further, Applicant respectfully notes that the Examiner has failed to address concerns related to improper hindsight reconstruction of the present invention.

New Claims

By way of this reply, new claims 14-17 have been added to the present application. New claim 14 requires an apparatus for simulating an anti-resonance circuit of a section of a microprocessor, comprising a processor, memory, and instructions residing in the memory and executable by the processor, the instructions to (i) simulate a load of the anti-resonance circuit with a simulated resistor, (ii) simulate a high-frequency capacitance of the anti-resonance circuit with a simulated transistor connected in parallel with the simulated resistor, and (iii) simulate an intrinsic capacitance of a section of the microprocessor with a simulated capacitor connected in parallel with the simulated resistor. Claim 15 requires that the simulated resistor is a simulated voltage controlled resistor. Claim 16 requires that the anti-resonance circuit is simulated in synchronization with a simulated clock cycle. Claim 17 requires that the simulation of the anti-resonance circuit begins on a leading edge of the simulated clock cycle. No new

matter has been added by way of these claims, as support for these claims may be found, for example, in paragraphs [0034]-[0037] of the present application.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.065001; P5347).

Dated: April 14, 2005

Respectfully submitted,

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